WHAT IS CLAIMED IS:

1. A method of forming a dual-sided semiconductor device from a wafer, the wafer having a top surface, a bottom surface, and a dopant concentration, the method comprising the steps of:

forming a layer of masking material on the top surface of the wafer;

patterning the layer of masking material to form a first opening in the layer of masking material that exposes a first region on the top surface;

forming a first opening in the wafer and a doped region in the wafer between the first opening in the wafer and the bottom side after the layer of masking material has been patterned, the doped region having a top surface exposed by the first opening in the wafer, and a dopant concentration that is greater than the dopant concentration of the wafer;

forming a layer of conductive material to fill up the first opening in the wafer; and

planarizing the layer of conductive material to form a first conductive region directly over the doped region.

2. The method of claim 1 wherein

the layer of masking material is also formed on the bottom surface of the wafer,

the layer of masking material is patterned to form a second opening in the layer of masking material that exposes a second region on the bottom surface of the wafer, the first and second openings being substantially aligned,

a second opening is formed in the bottom side of the wafer, the doped region in the wafer being between the first and second openings in the wafer after the layer of masking material has been patterned, the doped region having a bottom surface exposed by the second opening in the wafer;

the layer of conductive material is formed to also fill up the second opening in the wafer; and

the layer of conductive material is also planarized to form a second conductive region directly below the doped region.

3. The method of claim 2 wherein the step of forming a first opening in the wafer and a doped region in the wafer includes the steps of:

introducing a dopant into the wafer through the first and second openings in the layer of masking material, the dopant extending continuously through the wafer from the first region to the second region, and forming a continuous region through the wafer that has a dopant concentration greater than a dopant concentration of the wafer; and

etching the first and second regions for a predetermined period of time after the dopant has been introduced to define the first opening in the top surface of the wafer, the second opening in the bottom surface of the wafer, and the doped region there between.

4. The method of claim 2 wherein the step of forming a first opening in the wafer and a doped region in the wafer includes the steps of:

introducing a dopant into the wafer through the first and second openings in the layer of masking material, the dopant extending continuously through the wafer from the first region to the second region;

removing the layer of masking material after the dopant has been introduced;

forming a protective layer on the top surface and the bottom surface of the wafer after the layer of masking material has been removed;

patterning the protective layer to form a first opening in the protective layer that exposes the first region of the top surface, and a second opening in the protective layer that exposes the second region of the bottom surface, the first and second openings in the protective layer being substantially aligned; and

etching the first and second regions for a predetermined period of time after the protective layer has been patterned to define the first opening in the top side of the wafer, the second opening in the bottom side of the wafer, and the doped region there between.

5. The method of claim 2 wherein the step of forming a first opening in the wafer and a doped region in the wafer includes the steps of:

etching the first and second regions for a predetermined period of time to define the first opening in the top surface of the wafer, the second opening in the bottom surface of the wafer, and a remaining region there between; and

introducing a dopant into the wafer through the first and second openings in the layer of masking material, the dopant extending continuously through the remaining region to form the doped region.

6. The method of claim 2 wherein the step of forming a first opening in the wafer and a doped region in the wafer includes the steps of:

etching the first and second regions for a predetermined period of time to define the first opening in the top surface of the wafer, the second opening in the bottom surface of the wafer, and a remaining region there between;

removing the layer of masking material after the etch has been completed;

forming a protective layer on the top surface and the bottom surface of the wafer after the layer of masking material has been removed;

patterning the protective layer to form a first opening in the protective layer that exposes a top surface of the remaining region, and a second opening in the protective layer that exposes a bottom surface of the remaining region, the first and second openings in the protective layer being substantially aligned; and

introducing a dopant into the wafer through the first and second openings in the protective layer, the dopant extending continuously through the remaining region.

7. The method of claim 2 and further comprising the step of forming a first diffusion barrier on the doped region and exposed regions of the wafer, wherein the layer of conductive material is formed

on the first diffusion barrier to fill up the first and second openings in the wafer.

8. The method of claim 2 and further comprising the step of forming a second diffusion barrier to surround the layer of conductive material in the first and second openings in the wafer.

9. The method of claim 2 and further comprising the step of forming a first device that contacts the first conductive region, and a second device that contacts the second conductive region.

10. The method of claim 1 wherein the doped region has a surface substantially planar with the bottom surface of the wafer.

11. The method of claim 10 wherein the step of forming a first opening in the wafer and a doped region in the wafer includes the steps of:

introducing a dopant into the wafer through the first opening in the layer of masking material, the dopant extending continuously through the wafer from the top surface of the wafer to the bottom surface of the wafer; and

etching the first region for a predetermined period of time after the dopant has been introduced to define the first opening in the top surface of the wafer, and the doped region between the first opening and the bottom surface of the wafer.

12. The method of claim 10 wherein the step of forming a first opening in the wafer and a doped region in the wafer includes the steps of:

etching the first region for a predetermined period of time to define the first opening in the top side of the wafer, and a remaining region between the first opening and the bottom surface; and

introducing a dopant into the wafer through the first opening in the layer of masking material, the dopant extending continuously through the remaining region to form the doped region.

13. The method of claim 10 and further comprising the step of forming a first device that contacts the first conductive region, and a second device that contacts the doped region.

14. The method of claim 10 and further comprising the step of forming a contact through the doped region to make an electrical connection with the first conductive region.

15. The method of claim 14 and further comprising the step of forming a first device that contacts the first conductive region, and a second device that contacts the contact.

16. A dual-sided semiconductor device formed on a wafer, the wafer having a top surface, a bottom surface, and a dopant concentration, the device comprising:

a doped region formed in the wafer, the doped region having a top surface, a bottom surface, and a dopant concentration greater than the wafer;

an upper conductive region formed in the wafer over the top surface of the doped region, the upper conductive region having a top surface substantially planar with the top surface of the wafer.

17. The device of claim 16 and further comprising a lower conductive region formed below the bottom surface of the doped region in the wafer, the lower conductive region having a bottom surface, the upper conductive region, the doped region, and the lower conductive region forming a column through the wafer that electrically connects the top surface of the wafer with the bottom surface of the wafer.

18. The device of claim 17 wherein when no current flows through the column, a voltage on the top surface of the upper conductive region has a value that is substantially equal to a voltage on the bottom surface of the lower conductive region.

19. The device of claim 17 wherein when a current flows through the column, a voltage on the top surface of the upper conductive region has a value that differs from a voltage on the bottom surface of the lower conductive region by a difference value, the difference value being defined by a magnitude of the current times a resistance of the column.

20. The device of claim 16 wherein the bottom surface of the doped region is substantially planar with the bottom surface of the wafer.